Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1.-16. (Cancelled).

17. (Previously Presented) A microwave/millimeter-wave monolithic integrated circuit device, comprising:

a silicon substrate;

a plurality of first mesa portions disposed over the substrate;

a plurality of second mesa portions disposed over the substrate;

a plurality of PIN diodes each including a PIN anode region, wherein each one of the plurality of PIN diodes is disposed over a respective one of the plurality of first mesa portions;

a plurality of Schottky diodes each including a Schottky anode region, wherein one of the plurality of Schottky diodes is disposed over a respective one of the plurality of second mesa portions; and

a passivation layer disposed over the substrate, the passivation layer substantially covering the plurality of PIN diodes, the plurality of Schottky diodes, the plurality of first mesa portions, and the plurality of second mesa portions, while providing access to at least the PIN anode regions and the Schottky anode regions,

wherein the PIN anode regions are substantially co-planar with the Schottky anode regions.

18. (Previously Presented) A microwave/millimeter-wave monolithic integrated

circuit device of claim 17 wherein the passivation layer comprises a low-loss glass passivation layer.

19. (Previously Presented) A microwave/millimeter-wave monolithic integrated circuit device of claim 17 wherein each of the Schottky anode regions include an epitaxial layer.

20. (Previously Presented) A microwave/millimeter-wave monolithic integrated circuit device of claim 19 wherein the epitaxial layer of each of the Schottky anode regions has a thickness of approximately 0.1 μm.

21. (Previously Presented) A microwave/millimeter-wave monolithic integrated circuit device, comprising:

a silicon substrate;

a first mesa portion and a second mesa portion, the first and second mesa portions being disposed over the substrate;

a PIN diode including a PIN anode region, the PIN diode being disposed over the first mesa portion;

a Schottky diode including a Schottky anode region, the Schottky diode being disposed over the second mesa portion; and

a passivation layer disposed over the substrate, the passivation layer substantially covering the PIN diode, the Schottky diode, the first mesa portion, and the second mesa portion, while providing access to at least the PIN anode region and the Schottky anode region,

wherein the PIN anode region is substantially co-planar with the Schottky anode region.

22. (Previously Presented) A microwave/millimeter-wave monolithic integrated circuit device of claim 21 wherein the passivation layer comprises a low-loss

glass passivation layer.

23. (Previously Presented) A microwave/millimeter-wave monolithic integrated circuit device of claim 21 wherein the Schottky anode region includes an epitaxial layer.

24. (Previously Presented) A microwave/millimeter-wave monolithic integrated circuit device of claim 23 wherein the epitaxial layer of the Schottky anode region has a thickness of approximately 0.1 μm.

25. (Previously Presented) A method of fabricating a microwave/millimeter-wave monolithic integrated circuit device including at least one PIN diode and at least one Schottky diode, the method comprising:

providing a silicon substrate;

forming at least one first mesa portion and at least one second mesa portion on the substrate;

forming the at least one PIN diode including a PIN anode in a PIN diode region of the substrate, the at least one PIN diode being formed on the at least one first mesa portion;

forming the at least one Schottky diode including a Schottky anode in a Schottky diode region of the substrate, the at least one Schottky diode being formed on the at least one second mesa portion, the Schottky anode being formed in approximately the same plane as the PIN anode; and

depositing a passivation layer on the substrate to substantially cover the at least one PIN diode, the at least one Schottky diode, the at least one first mesa portion, and the at least one second mesa portion while providing access to at least the PIN anode and the Schottky anode.

26. (Previously Presented) A method of claim 25 wherein the depositing step

includes depositing a low-loss glass passivation layer on the substrate.

27. (Previously Presented) A method of claim 25 wherein the forming the at least one first mesa portion and the at least one second mesa portion further includes performing a single anisotropic etching operation.

28. (Previously Presented) A method of claim 27 wherein the forming the at least one first mesa portion and the at least one second mesa portion further comprises: depositing a layer of silicon nitride on the PIN diode region and the Schottky diode region of the substrate; masking portions of the PIN diode region and the Schottky diode region that are to become the at least one first mesa portion and the at least one second mesa portion; etching the silicon nitride layer except in the masked portions of the PIN diode region and the Schottky diode region, and conducting the single anisotropic etching operation to form the at least one first mesa portion and the at least one second mesa portion on the substrate.

29. (Previously Presented) A method of claim 25 wherein forming the PIN diode including a PIN anode further comprises: etching an implant window for the PIN anode in the PIN diode region of the substrate while masking the Schottky diode region of the substrate; and implanting a dopant through the implant window for the PIN anode in the PIN diode region of the substrate while masking the Schottky diode region of the substrate.

30. (Previously Presented) A method of claim 25 wherein the forming the at least one Schottky diode including the Schottky anode further includes forming the Schottky anode subsequent to the deposition of the passivation layer.

31. (Previously Presented) A method of claim 30 wherein the forming the at

least one Schottky diode including the Schottky anode further includes forming an epitaxial layer of the Schottky anode in the Schottky diode region of the substrate by an ultra-high vacuum chemical vapor deposition process while masking the PIN diode region of the substrate.

32. (Previously Presented) A method of claim 31 the forming the at least one Schottky diode including the Schottky anode further comprises forming the epitaxial layer of the Schottky anode at a temperature less than a transition temperature of the passivation layer.